REMARKS

This response is intended as a full and complete response to the non-final Office Action mailed March 29, 2005. In the Office Action, the Examiner notes that claims 1-11 are pending, of which claims 1, 2, 4, 5, 7, 8, 10 and 11 are rejected and claims 3, 6 and 9 are objected to. Claims 1, 7 and 10 are being amended to more clearly define the invention and not in response to prior art.

In view of the following discussion, Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicant believes that all of these claims are now in allowable form.

REJECTIONS

35 U.S.C. §102

Claims 1, 2, 4, 5, 7, 8, 10 and 11

The Examiner has rejected claims 1, 2, 4, 5, 7, 8, 10 and 11 under 35 U.S.C. §102(b) as being anticipated by Trinh et al. (5,132,648, hereinafter "Trinh"). Applicant respectfully traverses the rejection.

The Examiner alleges that regarding claims 1, 7 and 10, Trinh discloses a network for distributing a power signal in an optoelectronic circuit and its method comprising all aspects of the Applicant's invention. Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984)(citing Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 U.S.P.Q. 193 (Fed. Cir. 1983)) (emphasis added). The Trinh reference fails to teach or suggest each and every element of the claimed invention, as arranged in the claim.

Independent claim 1, 7 and 10 recites features of Applicant's invention that Applicant considers to be inventive. In particular, independent claim 1 recites:

> "A network for distributing a power signal in an optoelectronic circuit, said network comprising:
> a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal

lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level;

means for coupling said power signal from a primary input to the common point of the first level; and

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of optical signal generating devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of optical signal generating devices is substantially equal."

With respect to at least claim 1, the Applicant, in the specification specifically recites:

"This invention relates generally to a power distribution network for optoelectronic circuits and more particularly, to a power distribution tree network for optoelectronic devices, such as vertical cavity surface emitting lasers (VCSELs)" (Specification, page 1, lines 4-7).

"Although voltage-drops are not typically an issue for digital circuits or for low-current analog circuits, they can have a dramatic effect on the output power of optoelectronic devices and, in particular, VCSELs. We note that maintaining precise bias voltage across a chip is typically not an issue with digital circuits because these circuits are designed to be resistant to fluctuations in the power supply. However, as will be understood by persons skilled in the art, a VCSEL, for example, has a very sharp dependence on the voltage across the device due to the so-called sharp light (output power)-versus-current characteristic of such devices. In particular, the combination of large current requirements for VCSELs and finite resistance of the power supply lines can lead to small power supply differences (e.g. bias voltages) to VCSELS in different parts of the array that result in the large differences in light output power" (See Specification, page 5, lines 20-31).

"Thus, to maintain a constant level of output power for each VCSEL in an array of VCSELs on an OE-VLSI chip it is particularly important to ensure (1) that the threshold currents and voltages of each VCSEL are identical (an OEVLSI chip fabrication issue) and (2) that each VCSEL in an array is biased identically (a circuit design issue). The latter, in turn, relies on maintaining a constant voltage and current bias across the VCSELs." (See Specification, page 6, lines 9-14).

The Applicant in the specification further discloses:

"an H-tree interconnected conductive pathway configuration is used for powering optoelectronic devices, such as VCSELs, on an OE-VLSI chip." (See Specification, page 7, line 31 to page 8, line 2).

It is clear from at least the portion of the Applicant's Specification depicted above that the invention of the Applicant is directed, at least In part, to a network distribution system and method in an optoelectronic circuit. On an optoelectronic circuit with vertical cavity surface emitting lasers, it is crucial that the bias voltages cross these lasers are substantially the same. Because a small change in input current leads to a large change in output power, the H-tree network allows for the power supplied by each of the terminal nodes to each of the plurality of devices to be substantially equal. As a result, the bias voltages across the lasers are substantially the same.

The Trinh reference discloses "a method and apparatus for transferring radio frequency and phase control signals between backplate support structure and monolithic microwave integrated circuit." (Trinh, column 1, lines 3-6).

Trinh further discloses:

> In FIG. 7, a single RF input/output line is shown being power divided into a series of successively subdivided RF transfer lines in the case of a transmit array, and combined with preceding RF transfer lines in the case of a receive array. This structure allows the RF signal to be efficiently transferred between a single signal line and the thousands of elements found in a typical array. For EHF applications, RF feed striplines are typically about 0.0005 inches thick and 0.016-0.030 inches wide to achieve a 40-50 ohms input/output line. A variety of junction structures can be employed for the power divider/combiner and for interfacing with the conductive vias, see below, as will be readily apparent to those skilled in the art. Junctions such as the Wilkinson Junction have been found useful to meet transfer needs or desired efficiencies at required bandwidth.
>
> The connections of the RF stripline conductors to the MMIC module 14 are provided by the conductive vias 92. The next adjacent ceramic layer 54 supports a second ground plane 74 to complete the overall RF stripline. The stripline is a low loss shielded structure in which susceptibility to external RF interference is minimized. RF coupling is typically less than -90 dB. This structure is also less susceptible to electromagnetic interference and electromagnetic coupling. (Trinh, column 10, lines17-43).

It is clearly evident from at least the disclosure of Trinh that the invention of Trinh is directed to manufacturing of large Monolithic Microwave Integrated Circuit arrays and not for optoelectronic circuit. It is concerned with the electromagnetic interference and electromagnetic coupling of the RF signals being transmitted to the thousands of elements typically found in an array. Trinh's invention uses "RF power distribution

structure and advanced fabrication and assembly techniques to eliminate individually fabricated RF feedthroughs" (abstract).

The Trinh reference is completely different from Applicant's invention, since the Trinh reference fails to teach, or even suggest an optoelectronic circuit controlling bias voltage at the optical signal generating devices. Rather, the Trinh merely discloses large monolithic microwave integrated circuit arrays and structure to eliminate individually fabricated RF feedthroughs. Therefore, the Trinh reference fails to teach each and every element of the claimed invention.

As such, Applicant submits that independent claim 1 is not anticipated and fully satisfies the requirements of 35 U.S.C. §102 and is patentable thereunder. Independent claims 7 and 10 recite similar features as recited in independent claim 1. As such, and for at least the same reasons as discussed above, the Applicant submits that independent claims 7 and 10 also are not anticipated and fully satisfy the requirements of 35 U.S.C. §102 and are patentable thereunder. Furthermore, claims 2, 4, 5, and 8 depend, either directly or indirectly, from independent claims 1, 7 and 10 and recite additional limitations thereof. As such and at least for the same reasons as discussed above, Applicant submits that these dependent claims are also not anticipated and fully satisfy the requirements under 35 U.S.C. §102 and are patentable thereunder. Therefore, Applicant respectfully requests that the rejections be withdrawn.

ALLOWABLE SUBJECT MATTER

The Examiner has indicated that claims 3, 6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for indicating the allowable subject matter with respect to these claims. However, in view of the arguments set forth herein, the Applicant believes base claims 1 and 7 (and all intervening claims) are in allowable form and, as such, the dependent claims 3, 6 and 9, as they stand, are in allowable condition. Therefore, Applicant respectfully requests that the foregoing objection to claims 3, 6 and 9 be withdrawn.

CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

Dated: 5/10/05

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